

What is claimed is:

- 1 1. A method of allocating a memory address space to a plurality of Peripheral
2 Component Interconnect (PCI) adapters coupled to a plurality of slots in a PCI bus, the
3 method comprising:
4 accessing configuration data associated with a slot identifier for each of
5 the plurality of slots to determine a memory range size associated with each slot;
6 and
7 non-uniformly allocating memory address ranges to the plurality of PCI
8 adapters based upon the memory range sizes associated with each slot.

1 2. A method of allocating memory addresses to a plurality of input/output (IO)
2 resources coupled to a plurality of IO endpoints in a memory mapped IO fabric, the
3 method comprising:

4 determining a location in the memory mapped IO fabric for each IO
5 endpoint among the plurality of endpoints; and
6 non-uniformly allocating memory address ranges to the plurality of IO
7 endpoints based upon the determined locations of the IO endpoints in the memory
8 mapped IO fabric.

1 3. The method of claim 2, wherein determining the location and non-uniformly
2 allocating memory address ranges are performed during initialization of the memory
3 mapped IO fabric.

1 4. The method of claim 3, wherein determining the location and non-uniformly
2 allocating memory address ranges are performed during initialization of a computer to
3 which the memory mapped IO fabric is coupled.

1 5. The method of claim 4, wherein the computer comprises a logically-partitioned
2 computer, and wherein determining the location and non-uniformly allocating memory
3 address ranges are performed by a partition manager in the logically-partitioned
4 computer.

1 6. The method of claim 2, wherein allocating memory address ranges to the
2 plurality of IO endpoints includes allocating differently sized memory address ranges to
3 first and second IO endpoints having the same connector type.

1 7. The method of claim 6, wherein the first and second IO endpoints each
2 comprise an IO slot, and wherein the connector types of the first and second IO endpoints
3 have the same data bus width.

1 8. The method of claim 2, wherein the memory mapped IO fabric comprises a
2 PCI-compatible fabric.

1 9. The method of claim 8, wherein the memory mapped IO fabric comprises at
2 least one PCI-compatible bus, wherein at least a subset of IO endpoints are IO slots
3 coupled to the PCI-compatible bus, and wherein the location of each IO slot is defined by
4 a slot identifier for such IO slot on the PCI-compatible bus.

1 10. The method of claim 8, wherein the memory mapped IO fabric comprises a
2 plurality of PCI-compatible buses, wherein at least a subset of IO endpoints are IO slots
3 coupled to the plurality of PCI-compatible buses, and wherein the location of each IO slot
4 is defined by a bus identifier for the PCI-compatible bus to which such IO slot is coupled,
5 and a slot identifier for such IO slot on the PCI-compatible bus to which such IO slot is
6 coupled.

1 11. The method of claim 10, wherein the memory mapped IO fabric comprises a
2 plurality of IO enclosures, each IO enclosure including at least one PCI-compatible bus
3 among the plurality of PCI-compatible buses, wherein determining the location of an IO
4 endpoint comprises accessing configuration data associated with the IO enclosure within
5 which such IO endpoint is disposed.

1 12. The method of claim 10, wherein a PCI-compatible bus among the plurality
2 of PCI-compatible buses includes a PCI-compatible host bridge, the method further
3 comprising allocating a memory address range to the PCI-compatible host bridge,
4 wherein non-uniformly allocating memory address ranges to the plurality of IO endpoints
5 includes allocating memory address ranges to a plurality of IO slots coupled to the PCI-
6 compatible host bridge from the memory address range allocated to the PCI-compatible
7 host bridge.

1 13. The method of claim 12, wherein non-uniformly allocating memory address
2 ranges to the plurality of IO slots includes allocating a remaining memory address range
3 to a last IO slot among the plurality of IO slots, wherein the remaining memory address
4 range comprises that portion of the memory address range allocated to the PCI-
5 compatible host that was not allocated to each other IO slot among the plurality of IO
6 slots.

1 14. The method of claim 2, wherein the IO fabric includes at least one IO fabric
2 element allowing connectivity to a subset of the plurality of IO endpoints, and wherein
3 the memory address ranges that would be allocated to IO resources coupled to each IO
4 endpoint in the plurality of IO endpoints are determinable from a publication available
5 prior to installation of IO resources in the subset of IO endpoints.

1 15. An apparatus, comprising:

2 at least one processor;

3 program code configured to be executed by the at least one processor to
4 allocate memory address space to a plurality of input/output (IO) resources
5 coupled to a plurality of IO endpoints in a memory mapped IO fabric by
6 determining a location in the memory mapped IO fabric for each IO endpoint
7 among the plurality of endpoints, and non-uniformly allocating memory address
8 ranges to the plurality of IO endpoints based upon the determined locations of the
9 IO endpoints in the memory mapped IO fabric.

1 16. The apparatus of claim 15, wherein the program code is configured to
2 determine the location and non-uniformly allocate memory address ranges during
3 initialization of the memory mapped IO fabric.

1 17. The apparatus of claim 16, wherein the program code is configured to
2 determine the location and non-uniformly allocate memory address ranges during
3 initialization of the apparatus.

1 18. The apparatus of claim 17, wherein the apparatus comprises a logically-
2 partitioned computer, and wherein the program code is resident in a partition manager in
3 the logically-partitioned computer.

1 19. The apparatus of claim 15, wherein the program code is configured to allocate
2 memory address ranges to the plurality of IO endpoints by allocating differently sized
3 memory address ranges to first and second IO endpoints having the same connector type.

1 20. The apparatus of claim 19, wherein the first and second IO endpoints each
2 comprise an IO slot, and wherein the connector types of the first and second IO endpoints
3 have the same data bus width.

1 21. The apparatus of claim 15, wherein the memory mapped IO fabric comprises
2 a PCI-compatible fabric.

1 22. The apparatus of claim 21, wherein the memory mapped IO fabric comprises
2 at least one PCI-compatible bus, wherein at least a subset of IO endpoints are IO slots
3 coupled to the PCI-compatible bus, and wherein the location of each IO slot is defined by
4 a slot identifier for such IO slot on the PCI-compatible bus.

1 23. The apparatus of claim 21, wherein the memory mapped IO fabric comprises
2 a plurality of PCI-compatible buses, wherein at least a subset of IO endpoints are IO slots
3 coupled to the plurality of PCI-compatible buses, and wherein the location of each IO slot
4 is defined by a bus identifier for the PCI-compatible bus to which such IO slot is coupled,
5 and a slot identifier for such IO slot on the PCI-compatible bus to which such IO slot is
6 coupled.

1 24. The apparatus of claim 23, wherein the memory mapped IO fabric comprises
2 a plurality of IO enclosures, each IO enclosure including at least one PCI-compatible bus
3 among the plurality of PCI-compatible buses, wherein the program code is configured to
4 determine the location of an IO endpoint by accessing configuration data associated with
5 the IO enclosure within which such IO endpoint is disposed.

1 25. The apparatus of claim 24, wherein the configuration data associated with a
2 first IO enclosure among the plurality of IO enclosures is stored in non-volatile memory
3 resident in the first IO enclosure.

1 26. The apparatus of claim 23, wherein a PCI-compatible bus among the plurality
2 of PCI-compatible buses includes a PCI-compatible host bridge, wherein the program
3 code is further configured to allocate a memory address range to the PCI-compatible host
4 bridge, and wherein the program code is configured to non-uniformly allocate memory

5 address ranges to the plurality of IO endpoints by allocating memory address ranges to a
6 plurality of IO slots coupled to the PCI-compatible host bridge from the memory address
7 range allocated to the PCI-compatible host bridge.

1 27. The apparatus of claim 26, wherein the program code is configured to non-
2 uniformly allocate memory address ranges to the plurality of IO slots by allocating a
3 remaining memory address range to a last IO slot among the plurality of IO slots, wherein
4 the remaining memory address range comprises that portion of the memory address range
5 allocated to the PCI-compatible host that was not allocated to each other IO slot among
6 the plurality of IO slots.

1 28. The apparatus of claim 15, wherein the IO fabric includes at least one IO
2 fabric element allowing connectivity to a subset of the plurality of IO endpoints, and
3 wherein the memory address ranges that would be allocated to IO resources coupled to
4 each IO endpoint in the plurality of IO endpoints are determinable from a publication
5 available prior to installation of IO resources in the subset of IO endpoints.

1 29. The apparatus of claim 15, further comprising the plurality of IO resources
2 and the memory mapped IO fabric.

1 30. A program product, comprising:

2 program code configured to allocate a memory address space to a plurality
3 of input/output (IO) resources coupled to a plurality of IO endpoints in a memory
4 mapped IO fabric by determining a location in the memory mapped IO fabric for
5 each IO endpoint among the plurality of endpoints, and non-uniformly allocating
6 memory address ranges to the plurality of IO endpoints based upon the determined
7 locations of the IO endpoints in the memory mapped IO fabric; and
8 a computer readable signal bearing medium bearing the program code.

1 31. The program product of claim 30, wherein the computer readable signal
2 bearing medium includes at least one of a transmission medium and a recordable
3 medium.